

A Unified Hardware Accelerator for Fast Fourier Transform and Number Theoretic Transform

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Abstract—The Number Theoretic Transform (NTT) is an indispensable tool for computing efficient polynomial multiplications in post-quantum lattice-based cryptography. It has strong resemblance with the Fast Fourier Transform (FFT), which is the most widely used algorithm in digital signal processing. In this work, we demonstrate a unified hardware accelerator supporting both 512-point complex FFT as well as 256-point NTT for the recently standardized NIST post-quantum key encapsulation and digital signature algorithms ML-KEM and ML-DSA respectively. Our proposed architecture effectively utilizes the arithmetic circuitry required for complex FFT, and the only additional circuits required are for modular reduction along with modifications in the control logic. Our implementation achieves performance comparable to state-of-the-art ML-KEM / ML-DSA NTT accelerators on FPGA, thus demonstrating how an FFT accelerator can be augmented to support NTT and the unified hardware can be used for both digital signal processing and post-quantum lattice-based cryptography applications.

Index Terms—post-quantum cryptography, Number Theoretic Transform (NTT), Fast Fourier Transform (FFT), FPGA.

I. INTRODUCTION

Modern public key cryptography, based on the intractability of integer factorization and discrete logarithms, is vulnerable to future quantum adversaries capable of realizing Shor’s algorithm [1] in large-scale fault-tolerant quantum computers. Therefore, recent advances in quantum computing technologies have motivated the design and implementation of new quantum-secure cryptographic algorithms, also known as *post-quantum cryptography*. The U.S. National Institute of Standards and Technology (NIST) has been driving the standardization of post-quantum cryptography (PQC) since 2016 [2]. After several rounds of theoretical analysis, security evaluation and optimized implementation [3]–[5], NIST has selected CRYSTALS-Kyber [6] and CRYSTALS-Dilithium [7] as its primary recommendations for quantum-secure key encapsulation mechanism (KEM) and digital signature algorithm (DSA) respectively. These algorithms have also been included in the recently announced NIST PQC standards ML-KEM [8] and ML-DSA [9] respectively.

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Both ML-KEM (Kyber) and ML-DSA (Dilithium) are lattice-based cryptographic algorithms based on the hardness of the Module-LWE (Learning With Errors) problem [10]. They involve the computation of several polynomial multiplications which can be efficiently implemented using the *Number Theoretic Transform* (NTT). The NTT is a generalization of the widely used *Fast Fourier Transform* (FFT) [11]. All arithmetic in NTT is performed with integers in a finite field, while FFT requires the use of complex numbers.

Previous work has presented hardware implementations of NTT using custom accelerators as well as re-purposing existing cryptographic co-processors [12]–[21]. However, there has been little work in exploring how FFT hardware can be enhanced to implement NTT. Recently, [22] has proposed a high-level synthesis framework for polynomial multiplication using pipelined FFT architectures.

In this work, we present the FPGA-based implementation of a unified hardware accelerator supporting fixed-point complex FFT along with NTT for ML-KEM and ML-DSA parameters. We leverage the similarity between FFT and NTT butterfly operations to demonstrate that a traditional fixed-point complex FFT hardware accelerator can be augmented to achieve ML-KEM and ML-DSA NTT performance comparable to state-of-the-art custom NTT accelerators at the cost of $\approx 62\%$ more LUTs, $\approx 26\%$ more FFs, and no additional DSPs and BRAMs compared to the baseline FFT. Our proposed unified architecture will enable digital communication systems, e.g., wireless sensor nodes, which use FFT accelerators for data processing, to efficiently upgrade their hardware and also support PQC NTT for quantum-secure cryptographic protocols such as key encapsulation and digital signature-based authentication.

II. BACKGROUND

The FFT is an efficient algorithm used to compute the discrete Fourier Transform of sequences in digital signal processing, e.g., conversion from time domain to frequency domain. Given an N -length sequence of complex numbers $\{x_0, x_1, \dots, x_{N-1}\}$, its FFT is given by another N -length sequence of complex numbers $\{X_0, X_1, \dots, X_{N-1}\}$ where

$$X_k = \sum_{m=0}^{N-1} x_m \omega_N^{mk} \text{ for } k \in \{0, 1, \dots, N-1\}$$

Here, $\omega_N = \exp(-2\pi j/N)$ is the N -th complex root of unity ($j = \sqrt{-1}$), and its powers ω_N^{mk} are known as twiddle factors.

Similarly, given a polynomial $a(x) \in \mathbb{Z}_q[x]/(x^N + 1)$ with coefficients $a(x) = (a_0, a_1, \dots, a_{N-1})$, its NTT representation is given by $\hat{a}(x) = (\hat{a}_0, \hat{a}_1, \dots, \hat{a}_{N-1})$ where

$$\hat{a}_k = \sum_{m=0}^{N-1} a_m \zeta_N^{mk} \bmod q \text{ for } k \in \{0, 1, \dots, N-1\}$$

Here, ζ_N is the N -th primitive root of unity in the ring \mathbb{Z}_q , that is, $\zeta_N^N = 1 \bmod q$ and $\zeta_N^k \neq 1 \bmod q$ for $k \neq N$, and its powers ζ_N^{mk} are also known as twiddle factors. The modulus q must be chosen to be a prime such that $q \equiv 1 \bmod N$ in order to have elements of order N . Furthermore, to support negative-wrapped convolution [12] for polynomial multiplication, the modulus must also satisfy $q \equiv 1 \bmod 2N$ so that both the N -th and $2N$ -th primitive roots of unity modulo q exist.

Both FFT and NTT algorithms exploit the cyclic properties of ω_N and ζ_N respectively to efficiently compute the transform using a series of *butterfly* operations. There are two butterfly configurations – Cooley-Tukey (or Decimation-in-Time) and Gentleman-Sande (or Decimation-in-Frequency). In this work, we implement the former which computes $(a \pm \omega \times b)$ and $(a \pm \zeta \times b) \bmod q$ for FFT and NTT respectively, where a and b are inputs to the butterfly, and ω and ζ denote the twiddle factors. The overall FFT or NTT computation requires $\frac{N}{2} \log_2 N$ butterflies equally distributed across $\log_2 N$ stages.

For ML-DSA (Dilithium), the NTT parameters are $N = 256$ and $q = 8380417 = 2^{23} - 2^{13} + 1$. Therefore, it involves NTT computation with 256 23-bit polynomial coefficients and $\zeta_N = 3073009$. For ML-KEM (Kyber), the NTT parameters are $N = 256$ and $q = 3329 = 13 \cdot 2^8 + 1$. However, $q \not\equiv 1 \bmod 2N$ in this case, so the input polynomial is interpreted as 128 pairs of coefficients. Therefore, it involves NTT computation with 128 pairs of 12-bit polynomial coefficients and $\zeta_N = 17$. Further mathematical details of Dilithium and Kyber NTTs are available in [7], [9] and [6], [8] respectively.

III. HARDWARE ARCHITECTURE

To implement our unified accelerator, we begin with the FFT hardware as baseline and then include additional logic to add support for ML-KEM and ML-DSA NTTs. In this work, we consider 512-point complex FFT with signed inputs in 32-bit fixed-point Q16.15 format, that is, each of real and imaginary parts has 1 sign bit, 16 integer bits and 15 fractional bits. The complex twiddle factors ω (where $|\omega| \leq 1$) are represented in 32-bit fixed-point Q1.30 format, that is each of real and imaginary parts has 1 sign bit, 1 integer bit and 30 fractional bits. All negative quantities are assumed to be stored in standard two's complement format. Now, the complex FFT butterfly expression can be expanded as:

$$\begin{aligned} a \pm \omega \times b &= (a_R + ja_I) \pm (\omega_R + j\omega_I) \times (b_R + jb_I) \\ &= (a_R \pm \omega_R b_R \mp \omega_I b_I) + j(a_I \pm \omega_R b_I \pm \omega_I b_R) \end{aligned}$$

where a_R , b_R and ω_R are the real parts of a , b and ω respectively, and a_I , b_I and ω_I are their complex parts respectively. This requires four 32-bit fixed-point multiplications and several additions / subtractions, as shown in Fig. 1a. The

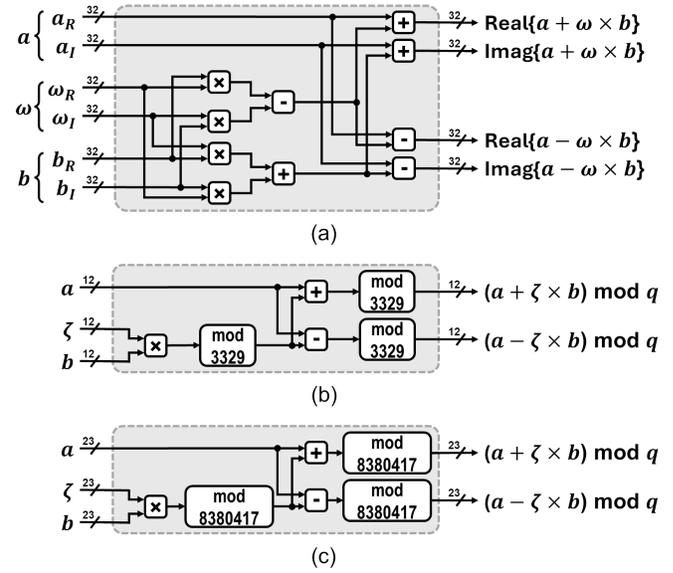


Fig. 1. Overview of butterfly computations in (a) FFT, (b) ML-KEM (CRYSTALS-Kyber) NTT and (c) ML-DSA (CRYSTALS-Dilithium) NTT.

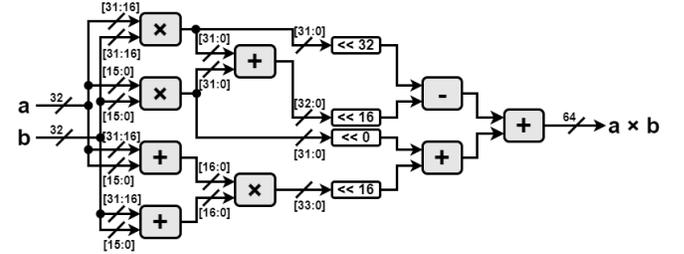


Fig. 2. Design of 32-bit Karatsuba multiplier using 16-bit multipliers.

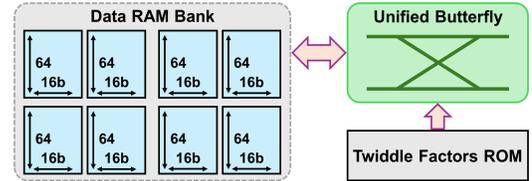


Fig. 3. Top-level architecture of the proposed unified accelerator.

complete 512-point FFT computation involves 9 stages with 256 butterflies per stage. Due the cyclic properties of twiddle factors, 512 complex signed 32-bit twiddle factors are required for the 512-point FFT computation.

Next, we analyze the computational requirements of ML-KEM and ML-DSA NTT butterfly operations. For ML-KEM butterfly $(a \pm \zeta \times b) \bmod q$, all inputs and outputs are unsigned 12-bit integers with arithmetic modulo $q = 3329$, as shown in Fig. 1b. Each ML-KEM NTT involves 7 stages with 64 pairs of identical butterflies per stage. Total 128 unsigned 12-bit integer twiddle factors are required for the NTT. For ML-DSA butterfly $(a \pm \zeta \times b) \bmod q$, all inputs and outputs are unsigned 23-bit integers with arithmetic modulo $q = 8380417$, as shown in Fig. 1c. Each ML-DSA NTT involves 8 stages with

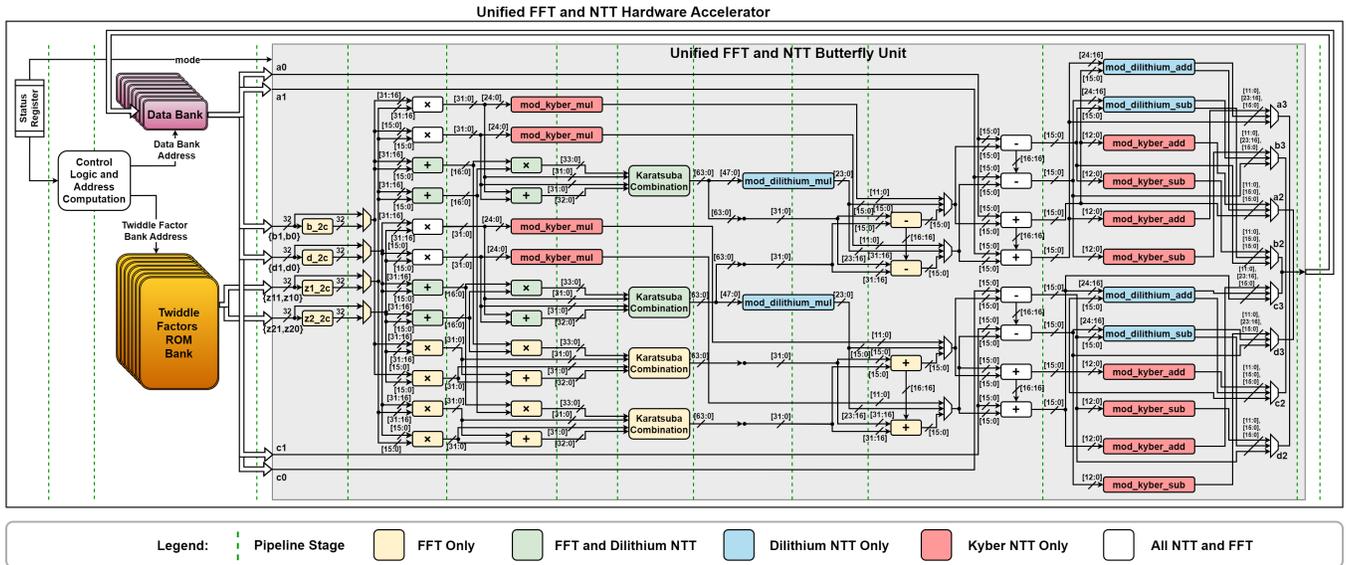


Fig. 4. Detailed architecture of the proposed unified butterfly unit and memory organization for FFT and ML-KEM (Kyber) + ML-DSA (Dilithium) NTT. The pipeline stages are shown as green dashed lines. The sub-modules of the unified butterfly unit used for FFT only, FFT + ML-DSA NTT, ML-DSA NTT only, ML-KEM NTT only and all NTT + FFT are shown in yellow, green, blue, red and white respectively.

128 butterflies per stage. Total 256 unsigned 23-bit integer twiddle factors are required for the NTT. We observe that ML-KEM NTT requires 12-bit multiplications while ML-DSA NTT requires 23-bit multiplications. Therefore, we effectively utilize the arithmetic circuits in the 32-bit fixed-point complex FFT by implementing its 32-bit multipliers in Karatsuba configuration [23] with several 16-bit multipliers, as shown in Fig. 2. Similarly, 32-bit additions / subtractions are split into pairs of 16-bit additions / subtractions with appropriate carry / borrow propagation logic. Butterfly inputs in ML-KEM and ML-DSA NTT are zero-padded to 16-bit and 32-bit respectively for the arithmetic operations. This approach requires no additional arithmetic modules except the modular reduction circuits specific to NTT. While Barrett reduction [24] is used to reduce the multiplication outputs, simple conditional subtraction / addition can be used to reduce the addition / subtraction outputs.

Finally, we analyze the memory organization required by the FFT and the two types of NTT. The FFT inputs are 512 complex numbers stored as 1024 elements of 32 bits each. The ML-KEM NTT inputs are 256 integers stored as 256 elements of 12 bits each. The ML-DSA inputs are 256 integers stored as 256 elements of 23 bits each. Therefore, ML-DSA elements can be accommodated in the same word size as FFT elements after zero padding to 32 bits, while pairs of ML-KEM elements can be accommodated in the same word size as single FFT elements after zero padding to pairs of 16 bits. Similar approach can also be followed for storing the FFT and NTT twiddle factors. Again, no additional memory is required to support NTT beyond the requirements of FFT.

The top-level architecture of the unified accelerator is shown in Fig. 3. Apart from the unified butterfly unit, it contains a data RAM bank, a twiddle factor ROM and control circuitry.

The butterfly inputs and outputs follow an in-place data flow. The data RAM bank is implemented as a set of eight 256×16 -bit true-dual-port memories. The twiddle factor ROM is implemented as a 1024×32 -bit dual-port read-only memory. The unified butterfly unit is implemented with a 9-stage internal pipeline for improved performance. It consists of four instances of the 32-bit unsigned Karatsuba multiplier described earlier. For signed multiplication in FFT, we include 32-bit and 64-bit two's complement converter circuits respectively before and after each 32-bit unsigned multiplier. Overall, our unified accelerator can execute either 1 FFT butterfly or 2 parallel ML-DSA NTT butterflies or 4 parallel ML-KEM NTT butterflies.

Detailed architecture of the accelerator with internal circuitry of the unified butterfly is shown in Fig. 4. It has three operating modes (indicated by a 2-bit external input): 512-point FFT, NTT for ML-KEM (CRYSTALS-Kyber) and NTT for ML-DSA (CRYSTALS-Dilithium). The 9-stage-pipelined unified butterfly arithmetic unit has twelve 16-bit inputs and eight 16-bit outputs. The mod_kyber_mul and mod_dilithium_mul units are used to perform Barrett reduction after multiplication in the NTT modes. The mod_kyber_add/sub and mod_dilithium_add/sub are used to reduce the addition/subtraction outputs in the NTT modes. Clearly, apart from modular reduction circuits and multiplexers, all other circuitry in the unified FFT + NTT butterfly unit are those already required for FFT, thus highlighting efficient hardware resource sharing in our proposed architecture.

IV. IMPLEMENTATION RESULTS

The proposed unified accelerator is implemented on a Xilinx Zynq UltraScale+ MPSoC ZCU104 Evaluation Board with an XCZU7EV-2FFVC1156E device [25] and our experimental setup is shown in Fig. 5. Verilog HDL (Hardware Description

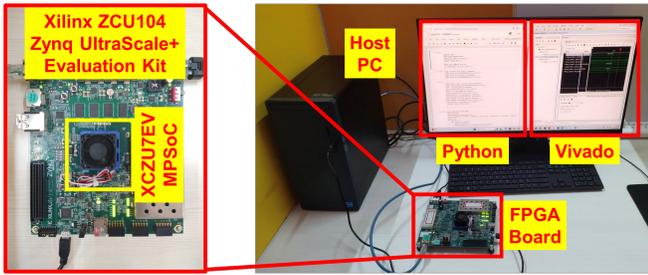


Fig. 5. Experimental validation setup with AMD Xilinx Zynq UltraScale+ ZCU104 MPSoC FPGA board and PYNQ interface.

TABLE I
ACCELERATOR IMPLEMENTATION RESULTS FROM ZCU104
(ZYNQ ULTRASCALE+ AT OPERATING FREQUENCY 400 MHz)

Design	Mode	LUT / FF / DSP / BRAM	Cycle Count	Latency (μ s)
I	ML-KEM	3716 / 2400 / 12 / 5	322	0.80
I	ML-DSA	3716 / 2400 / 12 / 5	624	1.56
I	FFT	3716 / 2400 / 12 / 5	2430	6.08
II	FFT	2300 / 1898 / 12 / 5	2430	6.08
III	ML-DSA	2287 / 1924 / 6 / 5	624	1.56
IV	ML-KEM	1973 / 1246 / 4 / 4.5	322	0.80
V	ML-KEM	3013 / 1828 / 6 / 5	322	0.80
V	ML-DSA	3013 / 1828 / 6 / 5	624	1.56

Language) is used to design the hardware accelerator, and Xilinx Vivado Design Suite version ML 2022.2 is utilized for FPGA synthesis, implementation and simulation. Our experimental validation framework interfaces the proposed accelerator with an additional bank of ROMs populated with test vectors corresponding to expected outputs at the end of all stages of the FFT or NTT computations. These test vectors are generated using a Python script based on the twiddle factors and random input sequences / polynomials. The validation framework also includes additional test logic to compare the data stored in the data RAM bank row-wise with the golden data stored in the ROMs. Five variants of the accelerator design are implemented: (I) FFT + ML-DSA NTT + ML-KEM NTT, (II) baseline FFT, (III) baseline ML-DSA, (IV) baseline ML-KEM, and (V) ML-DSA + ML-KEM. These are used to study the trade-offs associated with different levels of functional unification in the same underlying architecture. FPGA implementation results (resource utilization and performance metrics) for all five variants are shown in Table I.

Design II (our baseline FFT) follows the architectural blueprint of the Xilinx FFT IP [26]. Their primary difference is that Design II stores the inputs / outputs (4 KB) in 4 BRAMs compared to 2 BRAMs in [26], allowing multiple simultaneous reads / writes per cycle. We leverage this flexibility to get better performance metrics for our FFT baseline, as well as better architectural consistency with our NTT baselines, enabling fair comparison across design variants at the cost of higher BRAM usage. Compared to Design II, Design I (FFT + ML-DSA NTT + ML-KEM NTT) requires $\approx 62\%$ more LUTs and $\approx 26\%$ more FFs. The number of DSPs and BRAMs

remains unchanged. It is noteworthy that our careful design of the pipeline stages in the unified butterfly unit ensures that there is no reduction in the operating frequency (400 MHz for all the variants) due to the additional modular reduction circuitry. This shows the trade-off between additional NTT functionality and resource utilization. Compared to Design V (ML-KEM + ML-DSA), Design I requires 6 additional DSPs to accommodate two more 32-bit Karatsuba multipliers for FFT along with $\approx 23\%$ more LUTs and $\approx 31\%$ more FFs.

Table II compares our unified FFT + ML-KEM / ML-DSA NTT accelerator (Design I) with state-of-the-art FPGA-based NTT hardware accelerators for ML-KEM and/or ML-DSA. Despite supporting additional functionality, our implementation clearly achieves performance comparable to prior work in similar UltraScale+ FPGA platforms. The overheads in terms of LUTs, FFs, DSPs and BRAMs are primarily due to the additional circuitry for 512-point complex FFT which is not supported by any of the previous implementations. In particular, our unified accelerator requires 12 DSPs in order to support the fixed-point complex arithmetic for FFT and 5 BRAMs in order to store the complex inputs / outputs and twiddle factors for FFT. Our implementation demonstrates the efficiency and flexibility of the proposed unified FFT + NTT architecture which allows the same hardware to be used for both digital signal processing as well as post-quantum lattice-based cryptography applications.

V. CONCLUSIONS AND FUTURE WORK

The Number Theoretic Transform (NTT) is an indispensable tool for computing efficient polynomial multiplications in post-quantum lattice-based cryptography. It has strong resemblance with the Fast Fourier Transform (FFT) which is the most widely used algorithm for frequency-domain analysis of sequences in digital signal processing. Following this observation, we demonstrate a unified hardware accelerator supporting both 512-point complex FFT as well as 256-point NTT for NIST post-quantum cryptography standards ML-KEM and ML-DSA. Our proposed architecture effectively utilizes the arithmetic circuitry and memory organization required for FFT and re-purposes them for ML-KEM and ML-DSA NTT computations. Our FPGA-based implementations achieve performance comparable to state-of-the-art ML-KEM / ML-DSA NTT accelerators, thus demonstrating the efficiency of our design. Extension of our proposed architecture to support NTT for emerging applications of lattice-based cryptography such as homomorphic encryption [27] as well as efficient ASIC implementations will be explored in future work.

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TABLE II
COMPARISON WITH STATE-OF-THE-ART FPGA-BASED FFT, ML-KEM NTT AND ML-DSA NTT HARDWARE IMPLEMENTATIONS

Design	Supported Algorithms	FPGA Platform	FPGA Resource Utilization LUT / FF / DSP / BRAM	Mode	Freq. (MHz)	Cycle Count	Latency (μ s)
ISCAS '21 [15]	ML-KEM NTT only	Artix-7	609 / 640 / 2 / 2	ML-KEM	257	490	1.9
ARITH '21 [16]	ML-KEM NTT only	Artix-7	801 / 717 / 4 / 2	ML-KEM	222	324	1.46
CARDIS '22 [17]	ML-DSA NTT only	Artix-7	524 / 759 / 17 / 1	ML-DSA	311	533	1.71
TCAS-I '23 [18]	ML-DSA NTT only	Zynq UltraScale+	2759 / 2037 / 4 / 7	ML-DSA	391	—	—
TCAS-I '23 [19]	ML-KEM / ML-DSA NTT	Zynq UltraScale+	3487 / 1918 / 4 / 1	ML-KEM	270	—	—
				ML-DSA		—	—
TVLSI '24 [20]	ML-KEM NTT only	Kintex UltraScale	1914 / 2249 / 3 / 3	ML-KEM	275	—	—
	ML-DSA NTT only		5478 / 4955 / 12 / 6	ML-DSA	250	284	1.14
VLSID '24 [21]	ML-KEM / ML-DSA NTT	Zynq UltraScale+	2893 / 2356 / 4 / 4.5	ML-KEM	342	224	0.65
				ML-DSA		512	1.50
Xilinx FFT IP [26]	512-point Complex FFT only	Zynq UltraScale+	1462 / 2269 / 12 / 3	FFT	456	3548	7.78
This Work (Design I)	512-point Complex FFT + ML-KEM / ML-DSA NTT	Zynq UltraScale+	3716 / 2400 / 12 / 5	ML-KEM	400	322	0.80
				ML-DSA		624	1.56
				FFT		2430	6.08

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